UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,147	12/03/2003	Saverio Pezzini	02AG33853417	5293

27975 7590 12/19/2005

ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,147	PEZZINI, SAVERIO	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7 and 10-14* is/are rejected.

7)☒ Claim(s) *2-3, 8-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4-7, 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyer et al. (US Patent 6,449,676)

As per claim 1, Moyer discloses method of controlling interrupts generated by a peripheral, comprising:

- storing, in an interrupt pending register(fig.2, 58 ie interrupt pending register), active bits corresponding to interrupt flags(fig.2, 62 ie interrupt flag register) generated by said peripheral(fig.2, 50 ie interrupt sources); (col.3, lines 15-61, col.4, lines 21-34, ie bits stored in pending register are active bits which CPU determine from interrupt signals 42 or 43(sources) to be handle by reading the information contained in interrupt flag register provided to responding to the interrupts.)

- sending to an interrupt control circuit (fig.2, 81 ie ORing circuit) coupled to said peripheral an interrupt signal obtained by ORing said interrupt flags; (col.4, lines 43-67)
- upon receiving said interrupt signal(fig.2, 42 or 43 ie interrupt signals) said interrupt control circuit, identifying and serving the interrupt; (col.4, line 43-col.5, line 47)
- characterized in that it further comprises generating a respective bit string identifying an active bit corresponding to the interrupt that must be served; and (col.4, line 43-col.6, line 43), (col.3, lines 15-61, ie bits stored in pending register are active bits which CPU determine from interrupt signals 42 or 43(sources) has the highest priority to be handle by reading the information contained in interrupt flag register provided to responding to the interrupts.)
- serving the interrupt corresponding to said bit string. (col.5, lines 29-47), (col.3, lines 15-61, col.4, lines 21-34, ie bits stored in pending register are active bits which CPU determine from interrupt signals 42 or 43(sources) to be handle by reading the information contained in interrupt flag register provided to responding to the interrupts.)

As per claims 4, 10, Moyer discloses comprising the step of generating a third bit string identifying the number of active bits in said interrupt pending register of the peripheral that requested the interrupt. (co.6, lines 21-43 ie pending signal 92)

As per claim 5, Moyer discloses comprising the steps of: once the peripheral that generated the relative interrupt flag has been identified, copying the content of the interrupt pending register of the peripheral in an auxiliary register;(col.6, lines 1-43 ie interrupt flag register 62) and generating said bit string in function of the content of said auxiliary register. (col.6, lines 1-43)

As per claim 6, Moyer discloses an auxiliary interrupt control circuit, (fig.2, 10 ie data processing system) connectable to an interrupt control circuit(fig.2, 81 ie Oring circuit), to a microprocessor(fig.2, 12 ie cpu) and to at least a peripheral(fig.2, 50 ie interrupt sources) having an interrupt pending register(fig.2, 58 ie interrupt pending register), said control circuit receiving an interrupt signal corresponding to the logic OR of interrupt flags stored in said interrupt pending register, said auxiliary circuit comprising: (col.4, line 43-col.5, line 47)

an encoding circuit coupled to said interrupt pending register of the peripheral, sending to said microprocessor a bit string encoding the position of an active bit stored in said interrupt pending register corresponding to a certain interrupt to be served. (col.4, line 43-col.6, line 43), (col.3, lines 15-61, col.4, lines 21-34, ie bits stored in pending register are active bits which CPU determine from interrupt signals 42 or 43(sources) to be handle by reading the information contained in interrupt flag register provided to responding to the interrupts.)

As per claim 7, Moyer discloses the auxiliary circuit further comprising: an auxiliary register the size of which coincides to that of the interrupt pending register of the connected peripheral, for storing the content of said interrupt pending register; (col.4, line 43-col.5, line 47) said encoding circuit being coupled to said auxiliary register and said bit string encoding the position of an active bit stored in said auxiliary register. (col.4, line 43-col.6, line 43)

As per claim 11, Moyer discloses the auxiliary circuit further comprising an interrupt priority mask circuit, said first bit string encoding the position of an active bit corresponding to *a* pending interrupt of highest priority. (col.5, line 1-col.6, line 43 ie high order bits)

As per claim 12, Moyer discloses the auxiliary circuit further comprising a writable memory storing the priority values provided by said interrupt control circuit stored, said interrupt priority mask circuit depending on which peripheral generated an interrupt being configured in function of respective priority values stored in said writable memory. (col.5, line 1-col.6, line 43)

As per claim 13, Moyer discloses a peripheral(ie interrupt sources 50) connectable to a microprocessor (ie cpu 12) and to an interrupt control circuit(ie Oring circuit), associated to an interrupt pending register(ie interrupt pending register 58), said interrupt control circuit receiving an interrupt signal

corresponding to the logic OR of interrupt flags(ie interrupt flag register 62) generated by the peripheral and stored in said interrupt pending register, characterized in that it comprises an auxiliary control circuit. (col.4, line 43-col.6, line 43)

As per claim 14, Moyer discloses a microprocessor system, comprising an interrupt control circuit, a plurality of peripherals each being associated to a respective interrupt pending register, said control circuit receiving respective interrupt signals corresponding to the logic OR of interrupt flags stored in the respective interrupt pending register, a microprocessor coupled to said control circuit and to said peripherals, characterized in that it comprises: (col.4, line 43-col.6, line 43)

an auxiliary control circuit coupled to said peripherals and sending to said microprocessor a bit string encoding the position of an active bit stored in the interrupt pending register of the peripheral that generated the interrupt. (col.4, line 43-col.6, line 43)

3. Allowable Subject Matter

Claims 2 and 8, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's claimed invention is deemed allowable over the prior art of record as the prior art fails to teach or suggest wherein bit string identifies the position of the first active bit in said interrupt pending register of the peripheral that requested the interrupt.

Claims 3 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's claimed invention is deemed allowable over the prior art of record as the prior art fails to teach or suggest the method comprising the step of generating a second bit string identifying the position of the last active bit in said interrupt pending register of the peripheral that requested the interrupt.

Conclusion

4. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

November 13, 2005

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/12/05